



# Wirebondable Dual Value Thin Film Chip Resistor Networks, **Center Tap**



Actual Size

These tantalum chips combine excellent stability 0.07 % (2000 h, rated power at + 70 °C) with great power handling capacity. Two bonding pads per termination allow greater flexibility in hybrid layout design.

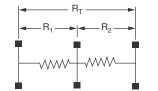
#### **FEATURES**

- · Center tap feature
- · Resistor material: Self-passivating Tantalum nitride
- Silicon substrate for good power dissipation
- Wirebondable
- · Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

**GREEN** 

(5-2008)

#### **SCHEMATIC**



STANDARD ELECTRICAL SPECIFICATIONS							
MODEL	SIZE	RESISTANCE RANGE <sup>(1)</sup> Ω	POWER RATING  P <sub>70 °C</sub> W	ABSOLUTE TOLERANCE ± %	RATIO TOLERANCE ± %	ABSOLUTE TCR <sup>(2)</sup> ± ppm/°C	RATIO TCR ± ppm/°C
TA 33	0303	50 to 1M	0.125	0.5, 1, 2	0.1, 0.5	50, 100	5

### Notes

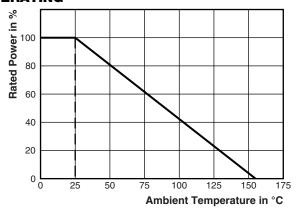
(1)  $(R_T = R_1 + R_2)$ 

 $<sup>^{(2)}</sup>$  ± 100 ppm/°C, ± 50 ppm/°C on request at - 55 °C to + 155 °C

PERFORMANCES					
TEST	SPECIFICATIONS	CONDITIONS			
Ohmic value: Ratio	1/1 standard (unequal values: please consult)				
Stability	± 0.07 % typical, ± 0.1 maximum	2000 h at + 70 °C under Pn			
Limiting voltage	50 V <sub>DC</sub> on R <sub>T</sub>				
Noise	< - 35 dB typical	MIL-STD-202 method 308			
Thermal EMF	0.01 μV/°C				
Shelf life stability	100 ppm	1 year at + 25 °C			

CLIMATIC SPECIFICATIONS				
Operating temperature range	- 55 °C to + 155 °C			
Storage temperature range	- 55 °C to + 155 °C			

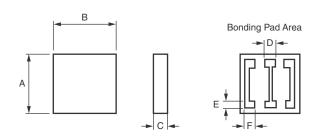
#### **DERATING**





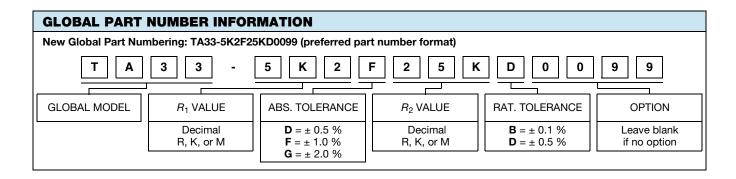
# Vishay Sfernice

### **DIMENSIONS**



DIMENSION	INCHES	MILLIMETERS	
Α	0.033 ± 0.004	0.855 ± 0.10	
В	0.033 ± 0.004	0.855 ± 0.10	
С	0.01 to 0.015	0.25 to 0.40	
D	0.006	0.15	
Е	0.004	0.10	
F	0.006	0.15	

MECHANICAL SPECIFICATIONS			
Resistive element	Tantalum nitride		
Substrate material	Silicon		
Passivation	Selfpassivation		
Bonding pads	Aluminum, gold on request		





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Vishay

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